



Docket No.: 67161-149

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of : Customer Number: 20277
Yasumasa TSUKAMOTO, et al. : Confirmation Number: 1709
Serial No.: 10/812,403 : Group Art Unit: 2818
Filed: March 30, 2004 : Examiner: Not yet assigned
For: SEMICONDUCTOR MEMORY DEVICE

**RESPONSE TO NOTICE
OF MISSING PARTS OF APPLICATION**

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Notice of Missing Parts of Application dated June 10, 2004, submitted herewith are the following documents for filing in the above-referenced application:

1. Declaration and Power of Attorney (which is in compliance with 37 CFR 1.63)
2. Statutory Basic filing fee of \$770.00
3. Late Filing Fee Surcharge of \$130.00
4. English Translation Surcharge of \$130.00
5. English Translation w/Verification
6. Replacement Formal Drawings
7. Preliminary Amendment w/attachments
8. Assignment and Recordation Fee of \$40.00 (on separate postcard)

10/812,403

Please charge Deposit Account No. 500417 in the amount of \$1030.00. To the extent necessary, Applicants petition for an extension of time under 37 C.F.R. 1.136.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

It is requested that the updated official filing receipt now be issued.

Respectfully submitted,

MCDERMOTT WILL & EMERY LLP


Stephen A. Becker
Registration No. 26,527

600 13th Street, N.W.
Washington, DC 20005-3096
202.756.8000 SAB:etp
Facsimile: 202.756.8087
Date: August 5, 2004



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of Yasumasa TSUKAMOTO and Koji NII

Serial No. 10/812,403

Filed: March 30, 2004

For: Semiconductor Memor Device

TRANSLATOR'S DECLARATION

Honorable Commissioner of Patents and Trademarks

Washington, D.C. 20231

Sir:

I, Yutaka Horii, certify that I am familiar with both the Japanese and the English language, that I have prepared the attached English translation of the Japanese patent application of Yasumasa TSUKAMOTO and Koji NII entitled Semiconductor Memory Device which was filed in the U.S. Patent and Trademark Office on March 30, 2004, and that the attached English translation is a true and complete translation of the corresponding Japanese language paper as originally filed.

I further declare that all statements made in this declaration of my own knowledge are true and that all statements made on information and belief are believed to be true; and further, that these statements were made with the knowledge that willful, false statements and the like so made are punishable by fine or imprisonment, or both, under § 1001 of Title 18 of the United States Code and that such willful, false statements may jeopardize the validity of legal decisions of any nature based on them.

Date: July 9, 2004



Yutaka Horii
Yutaka Horii